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IMPLEMENTATION OF A RECURSIVE DATA OF ADAPTIVE QRD-RLS ALGORITHM USING HDL CODER

Ali Khalid Jassim

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Abstract

Matrix inversion is a common function found in many algorithms used in wireless communication systems. As Field Programmable Gate Array (FPGA) become an increasingly attractive platform for wireless communication, it is important to understand the tradeoffs in designing a matrix inversion core on an FPGA. In this paper, a configurable Field Programmable Gate Array (FPGA)-based hardware architecture for matrix inversion is presented (download without data input). The proposed architecture of this algorithm has been design using Matlab-Simulink 7.8(R2009a) to deal with parallel structure. The design has been converted to behavioral VHDL coding style, as will as a VHDL test bench using Simulink HDL Coder tool to realize hardware directly from Simulink design. The use of Squared Givens rotations and a folded systolic array makes this architecture very suitable for FPGA implementation. Input is a 8×8 matrix of complex, floating point values. The matrix inversion design can achieve throughput of 0.14 M updates per second on a state of the art Altera Cyclone III (EP3C12F780C7) FPGA running at 125 MHz and studies a class of Q(N) approximate QR-based least squares (A-QR-LS) algorithm recently. It is shown that the A-QR-LS algorithm is equivalent to a normalized LMS algorithm with time-varying step sizes and element-wise normalization of the input signal vector.

Keywords and phrases: adaptive filtering, approximate QR-LS algorithm, performance analysis, QR-LMS algorithm, square root free givens based algorithms, transformed domain LMS algorithm.